initializing an internal circuit according to at least one from any of said power-on reset signals.

REMARKS

The Office Action dated April 22, 2002, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto. By this amendment, claims 2, 4 and 6 have been further amended to more clearly recite the subject matter of the claimed invention. The amendments made are merely cosmetic in nature. Claims 8-17 have been added. No new matter has been added by the amendments made herein. Therefore, claims 1-17 are pending in the present application and are respectfully submitted for consideration.

Claims 1-7 were rejected under 35 U.S.C. § 102(e) as being anticipated by Malherbe (U.S. Patent No. 6,252,442). Applicant submits that each of claims 1-7 recites subject matter that is neither disclosed nor suggested in the cited prior art.

In Malherbe, the power-on reset signal has a Low level when power is turned on, and a High level when the power is turned off, as shown in Fig. 1. Because of this, the power-on reset circuit of Malherbe does not pulse signals at the time power is turned on. However, in contrast, the power-on reset circuit of the present invention outputs pulse signals when the power is turned on, that is when the circuit is initialized. This happens because the present invention includes a main reset signal generating circuit, in addition to the sub reset signal generating circuit, as recited in claims 1, 3 and 5.

The power-on reset circuit in Malherbe appears to only be a circuit that can output the result of comparison between voltages. The control circuit in Malherbe (CE1-CEn) only makes a comparison between Vcc and the predetermined voltage (the

threshold voltage of the transistor), and outputs the result of the comparison.

Specifically, the power-on reset circuit in Fig. 3 of Malherbe includes a plurality of control circuits (CE1-CEn) and a composite circuit (OR). The reset signal (POR) that the power-on reset circuit outputs inhibits the operation of the internal circuit when Vcc is lower than Vs, and initiates the operation of the internal circuit when Vcc is higher than Vs, after power is turned on. As shown in Fig. 1, the internal circuit is operating when the reset signal (POR) is at a low level, a normal operation period, and the internal circuit operation is inhibited when the reset signal (POR) is not at a low level, a reset period.

For example, in the control circuit CE1 shown in Fig. 4 of Malherbe, the reset period by CE1 is decided by Vs1 when the threshold voltage of the P type transistor 10 is Vs1. Thus, when Vcc is lower than Vs1, the connecting node 1 of the P type transistor 10 is resistor 11 is at a low level, and a high level signal is output from CE1. The period when the high level signals are output is the reset period. When Vcc is higher than Vs1, the connecting node 1 rises to a high level, and a low level signal is output from CE1. The internal circuit initiates operation according to this signal, and the reset period shifts to the normal operation period.

Additionally, in the control circuit CE2 shown in Fig. 4 of Malherbe, the reset period CE2 is decided by Vs2 when the threshold voltage of the N type transistor 20 is Vs2. Thus, when Vcc is lower than Vs2, the connecting node 2 of the N type transistor 20 and resistor 21 is at a high level, and a low level signal is output from CE1. The period when the low level signals are output is the reset period. When Vcc is higher than Vs2, the connecting node 2 lowers to a low level, and a high level signal is output

from CE2. The internal circuit initiates operation according to this signal, and the reset period shifts to the normal operation period.

In the present invention, the sub reset signal generators correspond to the control circuits in Malherbe (CE1-CEn). The output signal of the sub reset signal generator 10 shown in Fig. 1 of the present application is the signal that has the waveform (a) shown in Fig. 3, and the output signal of the sub reset signal generator 12 shown in Fig. 1 of the present application is the signal that has the waveform (e) shown in Fig. 3. The sub reset signal generator 10 and 12 shown in Fig. 2 outputs the result of comparison between Vcc and the predetermined voltage.

However, in the present invention, the result of the comparison, which is the signals output from the sub reset signal generator, is respectively input to the pulse generators (indicated as 16 and 18 in Fig. 1). These pulse generators are not disclosed in Malherbe. The signals output from the pulse generators are pulse signals having waveforms (d) and (f) in Fig. 3, and the power-on reset signal (POR) is generated by synthesizing these pulse signals.

Therefore, the power-on reset circuit in Malherbe and the power-on reset circuit in the present invention is clearly different from each other. The power-on reset circuit in Malherbe outputs the result of comparison as it is, and the power-on reset circuit in the present invention converts the result of the comparison into pulse signals and outputs them.

Thus, Malherbe fails to disclose or suggest, a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit,

according to at least one from any of said sub power-on reset signals and said external power-on reset signal, as recited in claims 1, 3 and 5.

Therefore, it is respectfully submitted that the Applicant's invention, as set forth in claims 1, 3 and 5 is not anticipated within the meaning of 35 U.S.C. § 102.

As for claims 2, 4 and 6, Applicant submits that each of these claims recites subject matter which is neither disclosed nor suggested by the cited prior art. In particular, each of these claims depends on independent claims 1, 3 and 5, respectively. Therefore, each of these claims incorporates each and every limitation recited within claims 1, 3 and 5, respectively therein. Therefore, Applicant submits that each of claims 2, 4 and 6 also recites subject matter which is neither disclosed nor suggested by Malherbe for at least the reasons set forth above with respect to claims 1, 3 and 5.

Claims 1-3, 5 and 7 were rejected under 35 U.S.C. § 102(e) as being anticipated by Crotty (U.S. Patent No. 6,078,201). Applicant submits that each of claims 1-3, 5 and 7 recites subject matter that is neither disclosed nor suggested in the cited prior art.

Crotty discloses a power-on reset circuit for dual supply voltages. Figure 2 of Crotty illustrates the power-on reset circuit 200, which includes a dual-voltage detection circuit 210 coupled to a first supply voltage terminal Vcc1, a second supply voltage terminal Vcc2, and a ground terminal. The dual-voltage detection circuit 210 determines whether supply voltage Vcc1 is greater than a first adequate voltage level Vad1 and in response outputs a first voltage detection signal VD1,. Circuitry coupled to second supply voltage terminal Vcc2 drives first voltage detection signal VD1 on output terminal 211. If first supply voltage Vcc1 is less than the first adequate voltage Vad1,

the dual-voltage detection circuit 210 drives first voltage detection signal VD1 to a power-off logic level. If the first supply voltage Vcc1 is greater than the first adequate voltage Vad 1, the dual-voltage detection circuit 210 drives the first voltage detection signal VD1 to a power-on logic level.

Applicant respectfully submits that each and every element recited within claims 1, 3, 5 and 7 of the present application is neither disclosed nor suggested by Crotty. In particular, Applicant respectfully submits that the power-on reset circuit and the method for initializing an integrated circuit as recited in the present application is clearly distinct from that which is illustrated in Crotty. Specifically, it is submitted that Crotty fails to disclose or suggest a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one from any one of the sub power-on reset signals. Although Crotty discloses a power-on reset circuit, Applicant submits that the power-on reset circuit of Crotty is distinguishable from the present invention because the power-on reset circuit of Crotty comprises two voltage detection circuits, two low pass filters, and a buffer circuit. More importantly, the power-on reset circuit of Crotty does not generate pulse signals as the main reset signal generator does in the present invention. In other words, the power-on reset circuit in Crotty is only for detecting noise from the voltage (VD1 and VD2) from the power detection circuits, rather than having the function of outputting pulse signals as claimed in the present invention. Accordingly, Applicant respectfully submits that Crotty fails to disclose or suggest each and every element recited within claims 1, 3, 5 and 7 of the present application.

As for claim 2, Applicant submits that claim 2 recites subject matter which is

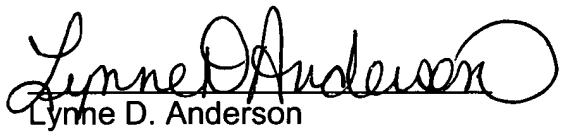
neither disclosed nor suggested by the cited prior art. In particular, claim 2 depends on independent claim 1, and therefore, incorporates each and every limitation recited within claim 1 therein. Therefore, Applicant submits that claim 2 also recites subject matter which is neither disclosed nor suggested by Crotty for at least the reasons set forth above with respect to claim 1.

Newly added claims 8-17 are also directed to a semiconductor integrated circuit having a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit. Therefore, it is respectfully submitted that claims 8-17 are also patentable over the applied references.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully submitted that the Examiner contact by telephone the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees, may be charged to counsel's Deposit Account No. 01-2300, **referencing Docket Number 108397-00025**.

Respectfully submitted,



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Enclosure: Marked-up version of claims
Petition for Extension of Time

MARKED-UP VERSION OF CLAIMS

Please amend claims 2, 4 and 6 as follows:

2. (Twice Amended) A semiconductor integrated circuit according to claim 1, wherein said main reset signal generator comprises:

a plurality of pulse generators for respectively generating pulses on the basis of a transition edge for a corresponding one of said sub power-on reset signals; and

a composite circuit for synthesizing the pulses to generate said main power-on reset signal.

4. (Twice Amended) A semiconductor integrated circuit according to claim 3, wherein said main reset signal generator comprises:

a plurality of pulse generators for respectively generating pulses on the basis of a transition edge for a corresponding one of said sub power-on reset signal and said external power-on reset signal; and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

6. (Twice Amended) A semiconductor integrated circuit according to claim 5, wherein said main reset signal generator comprises:

a plurality of pulse generators for respectively generating pulses on the basis of a transition edge for a corresponding one of said sub power-on reset signals and said external power-on reset signal; and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.